

S/N 09/945,507

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Leonard Forbes et al.	Examiner:	Unknown
Serial No.:	09/945,507	Group Art Unit:	2818
Filed:	August 30, 2001	Docket:	1303.014US1
Title:	FLASH MEMORY WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS		

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Account No. 19-0743 in order to have this Information Disclosure Statement considered.

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

LEONARD FORBES ET AL.

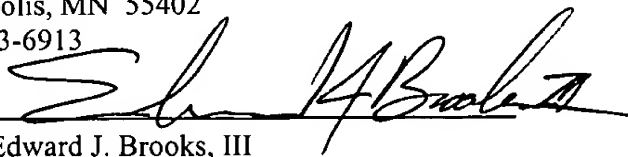
By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6913

Date

6/4/02

By



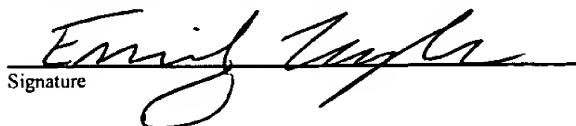
Edward J. Brooks, III
Reg. No. 40,925

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 4 day of June, 2002.

Name

Emily Legendre

Signature



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Applicant: Leonard Forbes et al.

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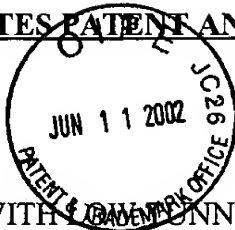
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Docket: 1303.014US1

Title: FLASH MEMORY WITH TUNNEL BARRIER INTERPOLY
INSULATORS



COMMUNICATION CONCERNING CO-PENDING APPLICATIONS

Commissioner for Patents
Washington, D.C. 20231

Applicant would like to bring to the Examiner's attention the following related pending applications in the above-identified patent application:

<u>Serial No.</u>	<u>Filing Date</u>	<u>Attorney Docket</u>	<u>Title</u>
08/902843	07/29/97	00303.354US1	DEAPROM HAVING AMORPHOUS SILICON CARBIDE GATE INSULATOR
08/903453	07/29/97	00303.378US1	CARBURIZED SILICON GATE INSULATORS FOR INTEGRATED CIRCUITS
09/134713	08/14/98	00303.354US3	DEAPROM HAVING AMORPHOUS SILICON CARBIDE GATE INSULATOR
09/135413	08/14/98	00303.354US2	DEAPROM HAVING AMORPHOUS SILICON CARBIDE GATE INSULATOR
09/256643	02/23/99	00303.324US2	TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND METHODS OF FABRICATION AND USE
09/258467	02/26/99	00303.378US2	CARBURIZED SILICON GATE INSULATORS FOR INTEGRATED CIRCUITS
09/650553	08/30/00	00303.378US3	CARBURIZED SILICON GATE INSULATORS FOR INTEGRATED CIRCUITS

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COMMUNICATION CONCERNING CO-PENDING APPLICATIONS

Serial Number: 09/945,507

Filing Date: August 30, 2001

Title: FLASH MEMORY WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS

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09/652420	08/31/00	00303.324US3	TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND METHODS OF FABRICATION AND USE
09/780169	02/09/01	01303.003US1	FLASH MEMORY WITH ULTRATHIN VERTICAL BODY TRANSISTORS
09/943134	08/30/01	01303.020US1	PROGRAMMABLE ARRAY LOGIC OR MEMORY DEVICES WITH ASYMMETRICAL TUNNEL BARRIERS
09/945395	08/30/01	01303.019US1	DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/945498	08/30/01	01303.024US1	DEAPROM WITH INSULATING METAL OXIDE INTERPOLY INSULATORS
09/945500	08/30/01	01303.029US1	PROGRAMMABLE MEMORY ADDRESS AND DECODE CIRCUITS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/945512	08/03/01	01303.027US1	IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/945514	08/03/01	01303.015US1	GRADED COMPOSITION GATE INSULATORS TO REDUCE TUNNELING BARRIERS IN FLASH MEMORY DEVICES

COMMUNICATION CONCERNING CO-PENDING APPLICATIONS

Serial Number: 09/945,507

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SRAM CELLS WITH REPRESSED
FLOATING GATE MEMORY, LOW
TUNNEL BARRIER INTERPOLY
INSULATORS

Respectfully submitted,

LEONARD FORBES ET AL.

By Applicant's Representatives,

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